Claims

1. A network topology backplane bus architecture comprising:

a plurality of independent data communication lines;

a plurality of processing nodes sharing said independent data communication lines for data communication;

one of said processing nodes transmitting and receiving on a first subset of said data communication lines and receiving on a second subset of said data communication lines; and

another of said processing nodes transmitting and receiving on said second subset ~~of said data~~ lines and receiving on ~~said first subset of said data lines.~~

2. The network topology backplane bus architecture recited in claim 1, wherein ones of said independent data communication lines comprise a first independent data communication network and different ones of said independent data communication lines comprise a second independent data communication network

3. The network topology backplane bus architecture recited in claim 2, wherein ones of said first subset of said data communication lines in combination with ones of said second subset of said data communication lines comprise one of said first and second independent data communication networks; and

different ones of said first subset of said data communication lines in combination with different ones of said second subset of said data communication lines comprise a different one of said first and second independent data communication networks

4. The network topology backplane bus architecture recited in claim 1, wherein said one of said processing nodes transmitting and receiving on a first subset of said data communication lines utilizes said first subset of said data communication lines for local communication within said processing node.

5. The network topology backplane bus architecture recited in claim 4, wherein said one of said processing nodes transmitting and receiving on a first subset of said data

communication lines further utilizes said first subset of said data communication lines for broadcasting transmissions to another of said processing nodes.

6. The network topology backplane bus architecture recited in claim 4, wherein said one of said processing nodes transmitting and receiving on a first subset of said data communication lines further utilizes said first subset of said data communication lines for receiving data transmissions from another of said processing nodes.

7. The network topology backplane bus architecture recited in claim 4, wherein said one of said processing nodes transmitting and receiving on a first subset of said data communication lines is one of a plurality of said processing nodes transmitting and receiving on said first subset of said data communication lines.

8. The network topology backplane bus architecture recited in claim 7, wherein each of plurality of processing nodes transmitting and receiving on said first subset of said data communication lines are co-located in a first resource enclosure.

9. The network topology backplane bus architecture recited in claim 7, wherein each of plurality of processing nodes transmitting and receiving on said first subset of said data communication lines time-shares said data communication lines with others of said plurality of processing nodes transmitting and receiving on said first subset of said data communication lines.

10. The network topology backplane bus architecture recited in claim 9, wherein each of plurality of processing nodes transmitting and receiving on said first subset of said data communication lines time-shares said data communication lines in synchronization with others of said plurality of processing nodes transmitting and receiving on said first subset of said data communication lines.

11. The network topology backplane bus architecture recited in claim 5, wherein said processing node transmitting and receiving on said second subset of said data lines and

receiving on said first subset of said data lines utilizes said second subset of said data communication lines for local communication within said processing node.

12. The network topology backplane bus architecture recited in claim 11, wherein said processing node transmitting and receiving on said second subset of said data communication lines further utilizes said second subset of said data communication lines for broadcasting transmissions to another of said processing nodes.

13. The network topology backplane bus architecture recited in claim 12, wherein ones of said processing nodes supports different ones of flight critical functions.

14. The network topology backplane bus architecture recited in claim 13, wherein one or more of said processing nodes supporting one of said flight critical functions is duplicated in one or more additional ones of said processing nodes.

15. The network topology backplane bus architecture recited in claim 14, wherein one of said processing nodes supporting said one of said flight critical functions is located in a first resource enclosure; and

at least one of said additional processing nodes supporting said one of said flight critical functions is located in a physically isolated second resource enclosure.

16. A network topology backplane bus architecture comprising:

a plurality of processing nodes transmitting and receiving data communications;

a plurality of independent data communication networks formed of a plurality of independent data communication lines, a subset of said data communication networks extending between ones of said plurality of processing nodes;

a first subset of ones of said data communication lines allocated to a first of said processing nodes for transmitting and receiving data communications, said first subset of said data communication lines further allocated to a second of said processing nodes for receiving data communications;

a second subset of ones of said data communication lines allocated to said second processing nodes for transmitting and receiving data communications, said second subset

of said data communication lines further allocated to said first processing nodes for receiving data communications.

17. The network topology backplane bus architecture recited in claim 16, wherein each of said plurality of processing nodes supports one or more processing functions.

18. The network topology backplane bus architecture recited in claim 17, wherein said first subset of said data communication lines comprises ones of said plurality of independent data communication lines forming each two or more of said plurality of independent data communication networks; and

said second subset of said data communication lines comprises different ones of said plurality of independent data communication lines forming each two or more of said plurality of independent data communication networks.

19. The network topology backplane bus architecture recited in claim 17, wherein said subset of said data communication networks extending between ones of said plurality of processing nodes comprises:

said first subset of ones of said data communication lines allocated to said first processing node for transmitting and receiving data communications; and

said second subset of ones of said data communication lines allocated to said second processing node for transmitting and receiving data communications.

20. The network topology backplane bus architecture recited in claim 19, wherein said first processing node is one of a plurality of first processing nodes each transmitting and receiving on said first subset of data communication lines; and

said second processing node is one of a plurality of second processing nodes each transmitting and receiving on said second subset of data communication lines.

21. The network topology backplane bus architecture recited in claim 20, wherein each of said plurality of first processing nodes are co-located in a first resource enclosure.

22. The network topology backplane bus architecture recited in claim 20, wherein each of said plurality of first processing nodes time-shares said data communication lines with others of said plurality of first processing nodes.

23. The network topology backplane bus architecture recited in claim 20, wherein one or more of said processing nodes supporting one of said processing functions is duplicated in one or more additional ones of said processing nodes.

24. The network topology backplane bus architecture recited in claim 23, wherein a first one of said processing nodes supporting said one of said processing functions is located in a first resource enclosure; and

at least one of said additional processing nodes supporting said one of said processing functions is physically isolated from said first one of said processing nodes in a second resource enclosure.

25. The network topology backplane bus architecture recited in claim 17, wherein said first subset of data communication lines allocated to a first of said processing nodes for transmitting and receiving data communications and said second subset of data communication lines allocated to said second processing node for transmitting and receiving data communications comprises a first of said data communication networks, said first data communication networks extending between ones of said plurality of processing nodes;

additional different ones of said plurality of independent data communication lines comprise a second of said data communication networks allocated to said first processing nodes for transmitting and receiving data communications among said first processing nodes; and

additional different ones of said plurality of independent data communication lines comprise a second of said data communication networks allocated to said second processing nodes for transmitting and receiving data communications among said second processing nodes.

26. The network topology backplane bus architecture recited in claim 25, wherein said first processing nodes comprise a single processing node supporting a first processing function; and

said second processing nodes comprise a single processing node supporting a second processing function.

27. The network topology backplane bus architecture recited in claim 26, wherein said first and second processing nodes are co-located in a single resource enclosure.

28. The network topology backplane bus architecture recited in claim 26, wherein said first and second processing nodes are located in respective first and second physically isolated resource enclosures.

29. The network topology backplane bus architecture recited in claim 26, wherein said first processing function and said second processing functions are essentially identical processing functions.

30. A method of sharing independent data communication lines for fault tolerant data communication among a plurality of processing nodes, the method comprising:

permitting to first processing nodes both transmitting and receiving privileges on a first subset of data communication lines and permitting receiving privileges to second processing nodes on said first subset of data communication lines;

permitting to the second processing nodes both transmitting and receiving privileges on said second subset of data communication lines and permitting receiving privileges to the first processing nodes on said second subset of data communication lines.

31. The method recited in claim 30, further comprising extending said first and second subsets of data communication lines between the first and second processing nodes.

32. The method recited in claim 31, further comprising isolating ones of said first subset of data communication lines and ones of said second subset of data communication

lines from other different ones of said first and second subsets of data communication lines.

33. The method recited in claim 30, wherein said first and second subsets of data communication lines comprise a single subset of inter-nodal data communication lines; and further comprising:

permitting both the first and second processing nodes to both transmit and receive on said inter-nodal data communication lines;

permitting the first processing nodes to both transmit and receive on a first additional subset of data communication lines; and

permitting the second processing nodes to both transmit and receive on a second additional subset of data communication lines.

34. A method of sharing independent data communication lines for fault tolerant data communication among a plurality of processing nodes, the method comprising:

permitting first processing nodes to both transmit and receive on a first subset of data communication lines and permitting the first processing nodes to receive on a second subset of data communication lines;

permitting second processing nodes to both transmit and receive on said second subset of data communication lines and permitting the second processing nodes to receive ~~on said first subset of data communication lines.~~